

# Designing low-power VLSI circuits: practical recipes

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The growing market of mobile, battery-powered electronic system demands the design of microelectronic circuits with low power dissipation. As the device size is drastically reducing, and density and complexity of the chips continue to enhance, the difficulty in providing adequate cooling might either add significant cost or limit the functionality of digital electronic systems which makes use of such integrated circuits. Power dissipation has become a critical design metric for an increasingly large number of VLSI (Very-large scale integration) circuits. The major challenges for design engineers are now to design new generation products that consume minimum power without compromising its performance or achieving minimum chip area as high speed and low power design as requirements for many applications. Modern chips consume ~100W of power of which about 20% is wasted in leakage through the transistor gates. The traditional means of

coping with increased power per generation has been to scale down the operating voltage of the chip but voltages are reaching limits due to thermal fluctuation effects. Several techniques, tools and methodologies for designing low power circuits have been already been observed in the scientific literature. However, only a limited number of such techniques, methodologies and tools have found their way in current design flows. Design a digital circuit for minimum transient energy consumption by eliminating hazards and glitch filtering by increasing inertial delay of gates or by inserting delay buffers when necessary is the current trend in low power VLSI circuit design. Several tricks may also be adapted during design to reduce power dissipation which will be presented at the talk.

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