

# Research on post-Si devices based on Ge and 2D channel materials and TCAD simulation

**Kazuhiko Endo**

National Institute of Advanced Industrial Science and Technology, Japan

The scaling limit of current CMOS technologies has been approaching rapidly. To further enhance performance of CMOS devices, advanced materials such as Ge and 2D materials are promising candidates. Advanced materials and devices integration group in AIST explore device integration technologies for going beyond the performance limit of Si CMOS. The research topics include Ge/III-V MOSFETs, 3D build-up integration, 2D channel materials and devices incorporating new materials and mechanisms such as spin FET and negative capacitance FET. We also focus on methodology and modeling of TCAD simulation and their application for various semiconductor devices. In this presentation, author will briefly introduce their current research activities. Recently, high-performance and low-power LSI is realized by miniaturization and scaling. However, as technology node approaches below 10 nm in 2020s, the end of the scaling is speculated. We are working on 3D build-up integration by vertical stacking of 2D circuits after the end of the scaling. For the stacking channel materials, we are focusing on both Ge and 2D-dichalcogenide materials. Ge substrate is one of the promising platforms for high-mobility channel transistors and photonic devices. We focus on high quality Ge platform by bonding epitaxially grown Ge layers to any substrates. Also, 2D-dichalcogenide materials attract much attention because of their unique characteristics. We focus on gas source Chemical Vapor Deposition of

2D-dichalcogenide and its 3D-stacked device application to realize beyond Si high-performance and low-power integrated circuits. In addition, the technology CAD (TCAD), a computer simulation for semiconductor manufacturing process and semiconductor device physics is very important for the post Si devices. We focus on methodology and modeling of TCAD simulation and their application for various semiconductor devices. We collaborate with other institutes in AIST to apply TCAD simulation for various devices and various projects and we also focus on industrial collaboration.

## Biography

Kazuhiko Endo is a Group Leader in the Advanced Materials and Devices Integration Group, Nanoelectronics Research Institute and National Institute of Advanced Industrial Science and Technology, Japan. He has completed his PhD in Electrical Engineering at the Waseda University in 1999. His research interests include nanometer scale manufacturing for aggressively scaled multi gate devices in advanced CMOS technologies. Prior to joining AIST, he was with Silicon Systems Research Laboratories, NEC Corporation from 1993 to 2003 where, he worked on the research and development of multilevel interconnects and high-k gate-stack technologies for ULSI. He was a Visiting Scholar at the Stanford University in 1999 and at the University of California Santa Barbara in 2015.

endo.k@aist.go.jp