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Integration of III-V nanowires on Si and their transistor applications

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Difficult issue for achieving ultralow power LSI is lowering supply voltage of FETs while overcoming physical limitation of sub threshold slope (SS=2.3 kBT/q=60 mV/dec). This limitation will stop further scaling of the power consumption even if multi gate architecture and III-V/Ge channels are implemented. The steep slope transistors such as tunnel FETs (TFETs) and negative capacitance FETs have therefore been proposed to overcome the limitation. The TFETs are most promising switching devices because of scalability for lower SS than 60 mV/dec and better compatibility with conventional integration process. However, there are some difficulties in decreasing SS while increasing on current as high as that of conventional FETs. Recently, we have successfully integrated vertical III-V nanowires on Si and Ge substrates by selective area growth. The important point for the heterogeneous integration was to modify the initial Si or Ge surfaces to (111) B-polar and we demonstrated high performance III-V NW based vertical FETs using modulation doped core multi shell layers. Beside the application, we proposed a new tunnel junction based on III-V/Si interface which is formed by selective area growth of III-V nanowires (NWs) on Si and demonstrated vertical TFETs with steep SS. This new tunnel junctions can inherently forms abrupt heterojunction regardless of precise doping because the band discontinuity is determined only by the offset of each III-V and Si. Thus, good gate electrostatic and depletion width controlling are defined only by the III-V channel region. In this presentation we report on recent progress in these heterogenous integrations of III-V nanowires on Si and Ge and device applications such as the vertical III-V NW FETs on Si/Ge and steep-slope TFETs using the III-V NW/Si heterojunctions. In TFET application, we present new approach of increasing tunneling current which is inherently low current. The new TFET using III-V NW/Si junction demonstrate rapid current enhancement and exhibit very high trans conductance efficiency which was much higher than the physical limitation of Si MOSFET-based analog integrated circuits.

Recent Publications

1. K. Tomioka, J. Motohisa, S. Hara, T. Fukui, Nano Letters, 2008, 8, 3475.
2. K. Tomioka, F. Ishizaka, T. Fukui, Nano Letters, 2015, 15, 7253.
3. K. Tomioka, M. Yoshimura, T. Fukui, Nature, 2012, 488, 189.

Biography

Katsuhiro Tomioka has completed his BE and MS degree in Electrical Engineering at Gunma University, Japan in 2003 and 2005 respectively and PhD in Electronics and Information Engineering at Hokkaido University, Sapporo, Japan in 2008. Since, 2016 June he is working as an Associate Professor at Hokkaido University. His current research area is on the formation of semiconductor nanowires and devices for future application to low power electrical switches and optical devices.

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