Design and Analysis of Full Adder Using Different Low Power Techniques

Mr. Bavusaheb kunchanur[1], Mrs. Swapna Srinivasan[2].

[1.] *M.Tech in VLSI design and embedded systems, MITE, Moodabidri.*

[2.] *Senior Assistant professor, MITE, Moodbidri.*

E-mail:- bavusaheb@gmail.com[1].

ABSTRACT

The complexity in VLSI design increases with an increase in the level of integration. Due to the portable electronics area, power and delay have become the most important factors. In conventional CMOS design, the area, power and delay are more compared to other Low power techniques. In this paper full adder is designed using different low power techniques, such as, conventional CMOS, GDI, Modified GDI and hybrid full adders which has a combination of GDI, TG, XOR, XNOR and pass transistor logic. All the designs are compared for area, power and delay. The power delay product graph is drawn for all the designs. The design and simulation are done in MENTOR GRAPHICS TOOL in 180 nm technology.

Keywords: low power, GDI, modified GDI, hybrid full adder, mentor graphics, PDP, full adder.

I INTRODUCTION:

The low power VLSI design is significant due to portable electronic products. The efficient way to reduce the power consumption is by reducing the threshold voltage and reduction in supply voltages. Adders are the building blocks in arithmetic operations such multiplication, division, subtraction, memory address calculation, Processors and DSP design. Since full adder is the basic block of binary adders. The performance of digital circuits is improved by enhancing the performance of full adder hence, it is attracting much attention of researchers. The various techniques have been reported and they all concentrated on reducing the area, power dissipation and delay. The transistor count of an adder will largely affect the complexity of many designs like ALU, multiplier and processors. The area and complexity can be reduced by reducing the transistor count. The speed depends on transistor size, delay in the critical path and parasitic capacitance. Different researchers used different techniques to reduce the delay, power and area[1][2][3][4]. Although they perform the similar function, each technique have their own advantages and disadvantages. Some of them used one logic style for the whole full adder[2][3][7] and others used a combination of different logic styles[5][6][8][9]. Here's one bit full adder is designed using different low power techniques such as, conventional CMOS, GDI, Modified GDI, 16T full adder, 14T full adder and 8T full adder and they are compared for area and power delay product.

II DESIGN AND COMPARATIVE ANALYSIS:

a) Conventional CMOS design: it is based on normal complementary metal oxide semiconductor design with P-MOS as pull-up and N-MOS pull-down transistor[1][3]. It has the advantages of very low power dissipation, but this design requires 28 transistors, thus the silicon area is more and the complexity is more for larger designs. Due to the low mobility of P-MOS block the speed is less compared to other logic designs. The design and simulation result for conventional CMOS 28T full adder is shown in Fig 1(a), and Fig1(b).

b) Gate Diffusion Input (GDI): The design consists of 2 XNOR gates designed by 4 transistors. The GDI full adder requires 10 transistors, which is very less compared to CMOS and the speed is more[2]. But the main drawback of GDI technique is it suffers from swing degradation due to threshold loss and it requires silicon on insulator or twin-well process to realize which is expensive to realize[7]. The GDI full adder design and simulation result is shown in the fig 2(a) and 2(b).

c) Modified GDI: P-MOS pass strong logic '1' and N-MOS pass strong logic '0'. In order to reduce the swing degradation problem in conventional GDI, an additional N-MOS is used in parallel to P-MOS with inverted gate input. This design requires 17 transistors to realize full adder. Although the transistor count is more compared to GDI technique, it will give accurate output and it has less power dissipation compared with GDI. The design and simulation for Mod GDI full adder is shown in the fig 3(a) and 3(b).

d) 16T Full Adder: The 16T full adder is shown in the fig 4(a). It is the combination of pass transistor logic, transmission gates and low power XOR, XNOR gates[8]. It requires 16 transistors and the power dissipation and delay are less compared to other alternative designs. But this design suffers from swing degradation due threshold loss. The simulation result is shown in the fig 4(b).

e) 14T Full Adder: This design is the combination of pass transistor logic and transmission gate logic[5]. The design is shown in fig 5(a), Here 4 transistor XOR and 6 transistor XNOR, are used to generate sum and carry [9]. The silicon area and delay are less compared to conventional CMOS design. The simulation result is shown in the fig 5(b)

III RESULT ANALYSIS AND CONCLUSION:

The comparison of different logic designs are shown in table 1.Which shows transistor count, power dissipation, delay and power delay product. From the analysis of different logic full adders it concludes that, the PDP of 16T full adder is very less but, it suffers from swing degradation. Although the modified GDI full adder has a little larger PDP compared to 16T but, it will give the proper output. The analysis concludes that, the modified GDI technique is the most efficient one for larger designs.

REFERENCES

1. Comparison of 1 Bit Low Power-High Speed Designs Leakage Minimization Full Adder, International Journal of Advanced Research in Computer Science and Software Engineering, Volume 4, Issue 10, October 2014.
2. Low power-area GDI & PTL techniques based full adder designs, ACITY, AIAA, CNSA, DPPR, NECOM, WEST, DMS, P2PTM, VLSI – 2013
3. Design and Implementation of 16-bit Ripple Carry Adder for Low Power in 45nm CMOS Technology, International Journal of Emerging Technology and Advanced Engineering (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 4, Issue 1, January 2014)
4. Design and Analysis of Low-Power 11-Transistor Full Adder, International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering (An ISO 3297:2007Certified Organization)Vol. 3, Issue 6, June 2014.

5. Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate, International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.4, December 2011.
6. Low power-area designs of 1bit full adder in cadence virtuoso platform, International Journal of VLSI design & Communication Systems (VLSICS) Vol.4, No.4, August 2013.
7. Design and Analysis of GDI Based Full Adder Circuit for Low Power Applications, Pankaj Kumar et al Int. Journal of Engineering Research and Applications www.ijera.com ISSN : 2248-9622, Vol. 4, Issue 3(Version 1), March 2014, pp.462-465.
8. A Novel 1-Bit Full Adder Design Using DCVSL XOR/XNOR Gate and Pass Transistor Multiplexers, International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-2, Issue-4, March 2013.
9. A New design of 1-bit full adder based on XOR-XNOR gate, International Journal of Enhanced Research in Science Technology & Engineering, ISSN: 2319-7463 Vol. 3 Issue 6, June-2014.

Table 1: comparison of power and delay for different logics

Parameters	CMOS	GDI	Mod GDI	16T	14T
Transistor count	28	10	17	16	14
Power(μw)	0.381	1.01	0.16	0.154	1.16
Delay(nS)	0.188	0.0971	0.131	0.0607	0.16
PDP(10^{-17})J	7.1628	9.8071	2.096	0.934	18.5

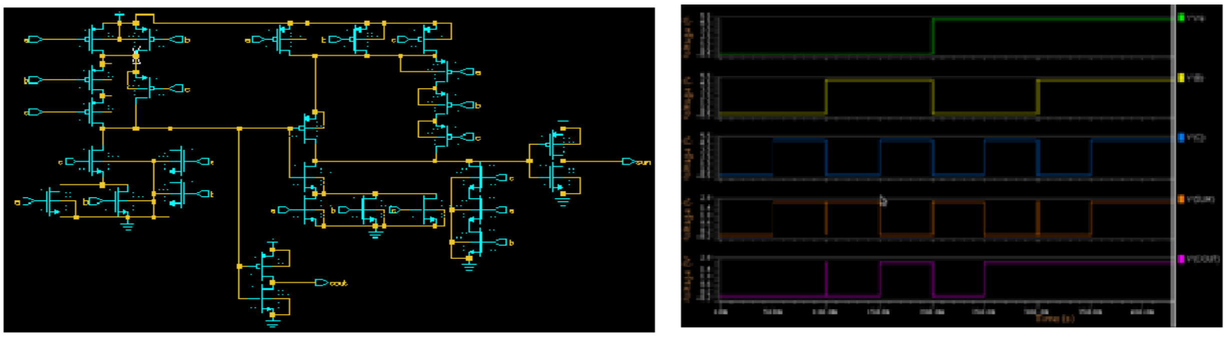

Fig 1(a)CMOS full adder with 28T and (b) Simulation result for 28T full adder

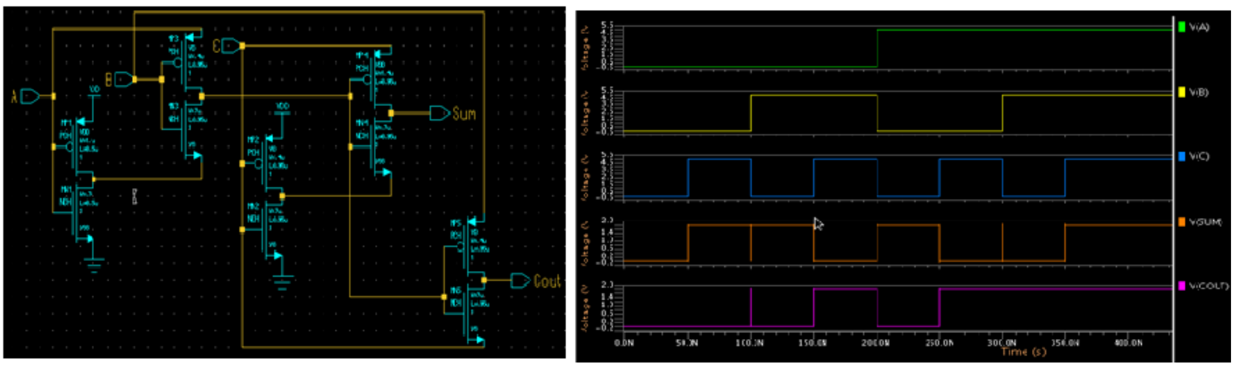

Fig 2 (a) Full adder using 10T GDI technique and (b) simulation result for GDI full adder

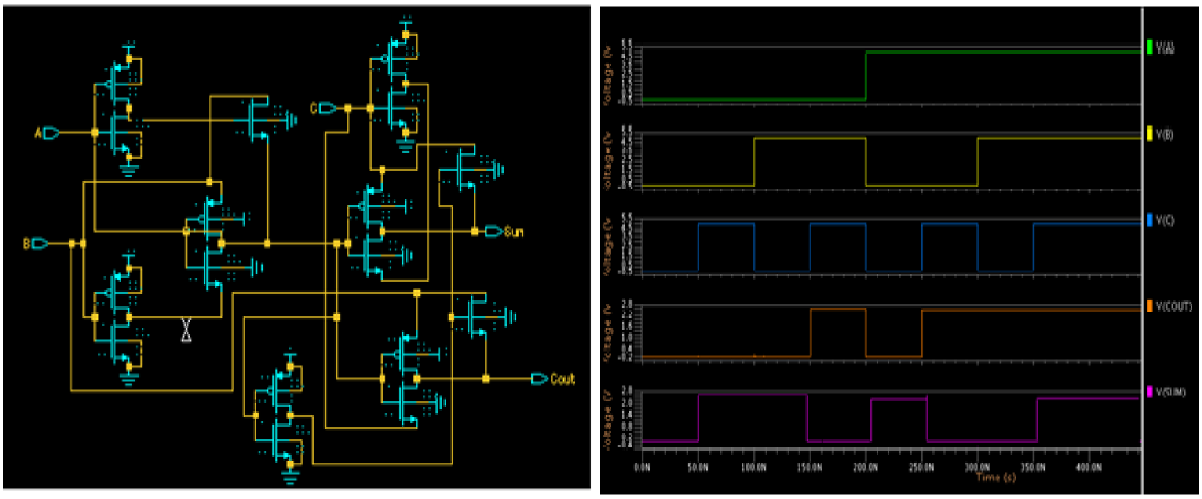

Fig 3(a) Modified full swing GDI full adder and (b) simulation result for modified GDI FA.

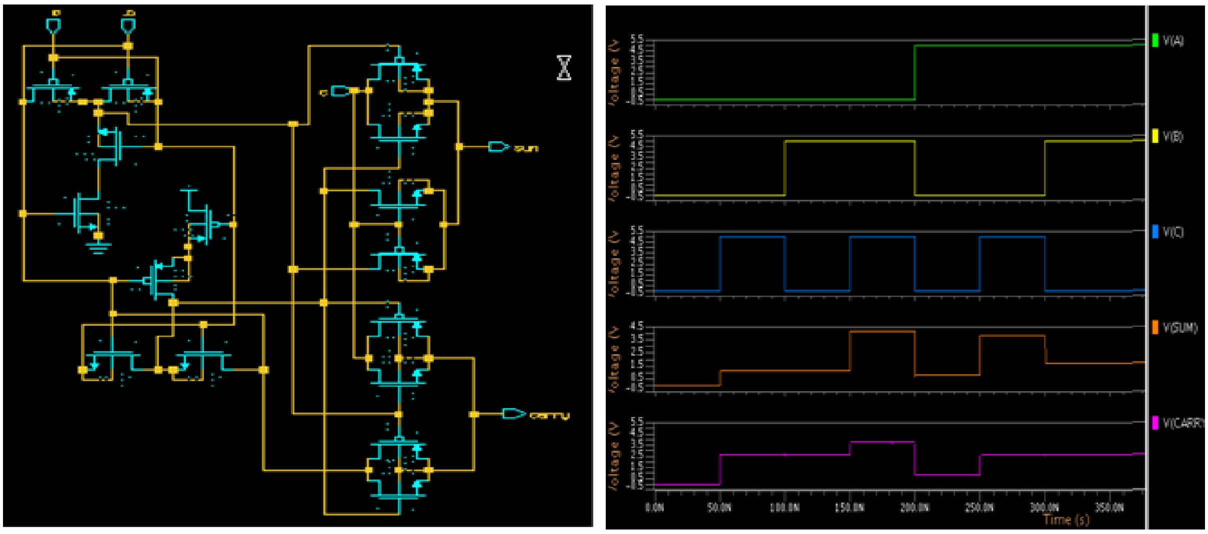

Fig 4(a)Full adder using 16 Transistors and (b) Simulation result for hybrid 16T full adder

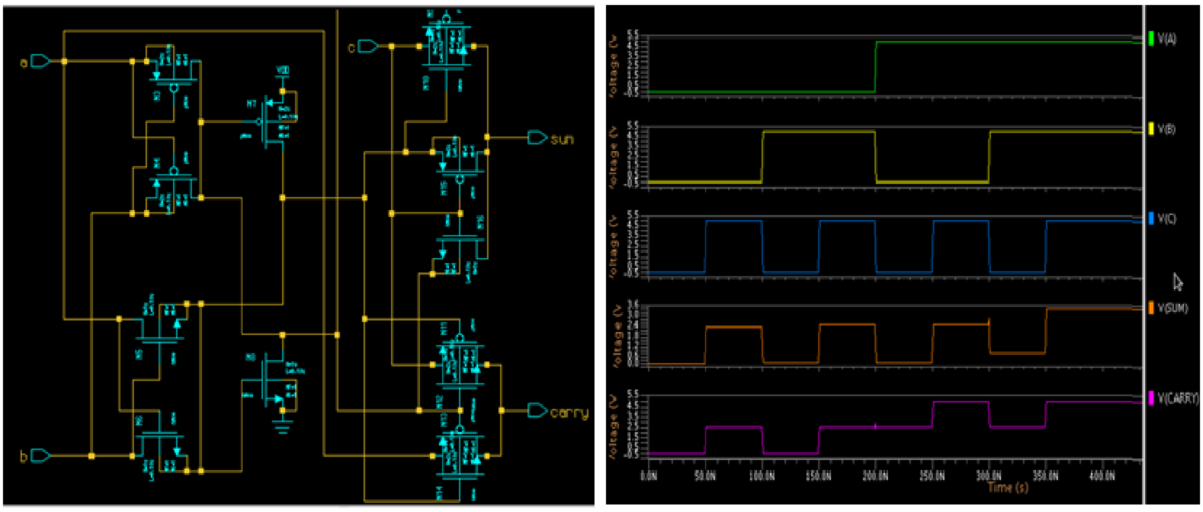

Fig 5(a) Hybrid full adder using 14Transistor and (b) Simulation result for hybrid 14T FA